Automated Speed Control using 32bit RISC-V

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*Abstract*—**An automated speed controller is developed which interprets the data and automatically reduces the speed during crowded path and can also bring a car to a halt when needed. This has been developed with the help of proper simulation software, yielding satisfactory result so far.**

Keywords— RISC-V, Sensors, Instructions, Simulation

# Introduction

Nowadays, as time is more and more constrained, drivers often drive erratically which frequently leads to mishaps. The engineering of the roads is also not up to the mark in most of the places and vehicle density has also increased significantly over the past decade. To overcome this problem, an automated speed controller is developed. Whenever an obstacle is detected, information is passed to the system which in turn controls the braking mechanism and thereby controlling the speed based on the calculated distance. The project is basically a 32-bit digital processor based on RISC-V, with the help of SPICE. Reduced Instruction Set Computer (RISC) architecture is such that the instruction set is optimized with a large number of registers and a highly regular instruction data path allowing a large number of clock cycles per instructions. The load-store architecture is a common feature in which memory is accessed through specific instructions rather than as a part of most instructions in the set. We will be simulating the entire scenario using real-life inspired conditions in a software named SUE and Cppsim view.

# Tools/Software

## SUE2

The entire schematics of the project are designed in SUE2 (Schematic User Environment 2) which is graphical user interface which enables user to design and get an architectural overview. It has schematic verification with verilog control, timing models and standard cell libraries. SUE2 can drill down to transistor level details and fully hierarchical.

## CppSimView

CppSimView comes along with SUE2 in same package. CppSimView shows the graphical visualization of the simulation data of the schematic created in SUE2. Data can see from various nodes by manually or predefined earlier

# Overview

Being the second most populated country in the world our nation faces the maximum number of accidents and accidental fatalities while comparing to other nations around the world. Road transport is a major type of transport system used in India. The Ministry of Road Transport & Highways report revealed that India has got one road accident every minute in a year which lost one life in 3 minutes. Contrary to popular belief, only 1.5% of the accidents are caused by defective roads. In the majority of the cases (77%), the driver is at fault. Surveys have shown that maximum rate of serious road accidents are raised due to high uncontrollable speed than necessary speed limited in the particular zone and also due to unaware obstacles. Therefore, minimizing the number of rate of accidents and their worst consequences is challengeable task for the car makers and traffic controllers. The driver needs to get aware by any means to stop the hazard. And this system is available in today's vehicle as a special feature in the vehicles market, and the future vehicle requires higher safety in driving controls intelligently in each and every vehicle. This becomes more dangerous in populated regions like schools or hospitals. In school areas, speed breakers are provided to reduce the speed of vehicles, but the drivers do this manually. Many times, due to driver’s fault speed is not controlled. Therefore, proper techniques need to be implemented using technology and its derivatives.

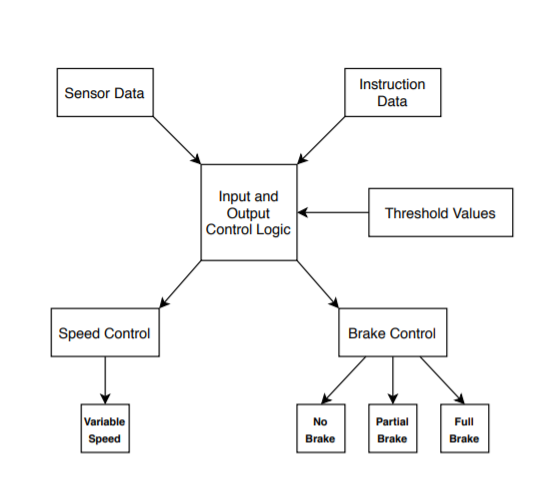
# Operations

Here we are discussing the operations of the digital processor built using SPICE

## Working

Information is received from 16-bit “far distance sensor” and “near distance sensor” which sets up five 32-bit instructions that are stored in their respective registers. The “near distance sensor” gives three values i.e., whether the near distance is HIGH, LOW or MEDIUM. The “far distance sensor” gives the value of how far the car is. The input control logic based on the program counter (PC) value, picks instructions and passes them on to the instruction register (IR), where they are saved for a given clock cycle and then processed. Basically, the PC will tell the input control logic which of these five instructions get passes to the IR. Based on the values, they are compared to the given set threshold. A part of the instruction from the IR is compared with threshold using a comparator and that output of the comparator is passed on to the output control logic and the rest of the instruction from the IR is also passed on to the output control logic. The output control logic sets two registers i.e., “speed register” and “braking register”, both are 16-bit values. These will control whether it will speed up the car or slow down the car or completely brake the car.

## Flowchart



## Output/Results

#### Speed Control

The speed control registers get constantly updated depending on the distance at which the other vehicles are travelling with the reference vehicle i.e. if the other vehicles are at far distance then speed data increase its value causing increase in speed and if other vehicles are near then speed value decrease resulting in reduction of speed.

#### Brake Control

Brake control has three different modes.

1. No brakes.
2. Partial brakes.
3. Full brakes.

No brake condition is always kept loaded on the braking register with a value of 000FH

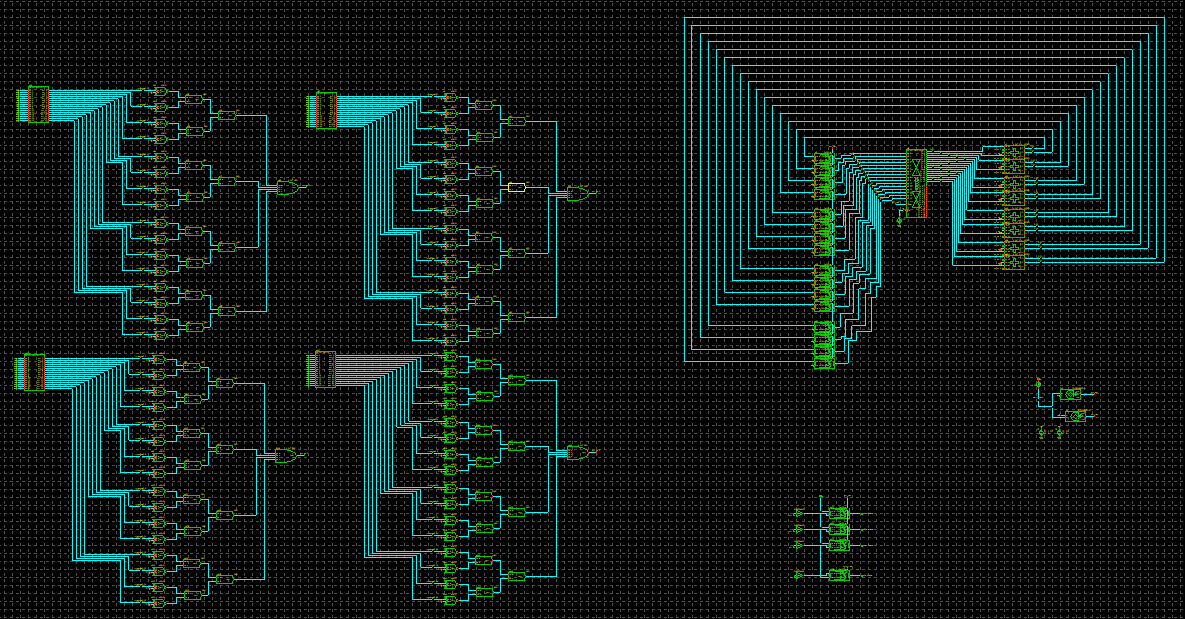
Partial brake is loaded when data in braking register is updated to 00F0H after data enable is pulled high causing vehicle to slowdown.

Full brakes are applied when braking register attain 0F00H value after data enable is pulled high causing complete reset of speed register and halt of vehicle

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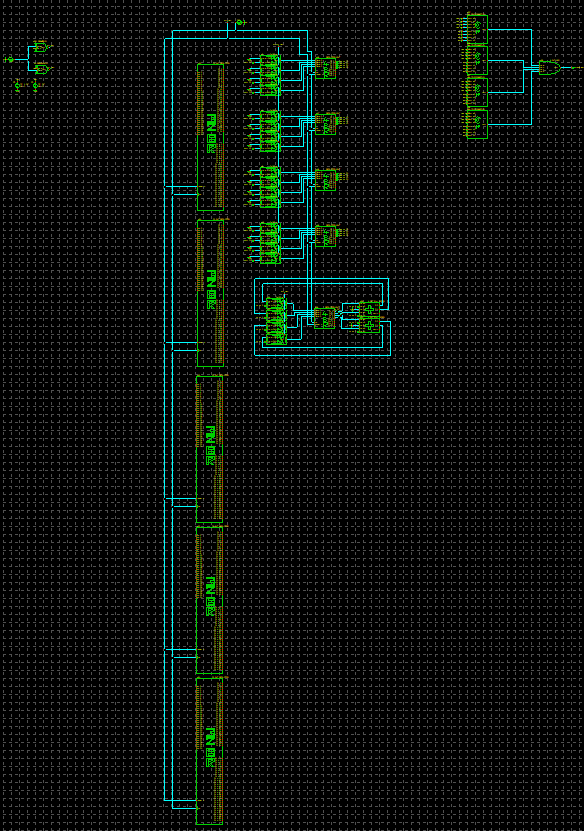


Figure: SUE2 schematic of the processor.

OUTPUTS

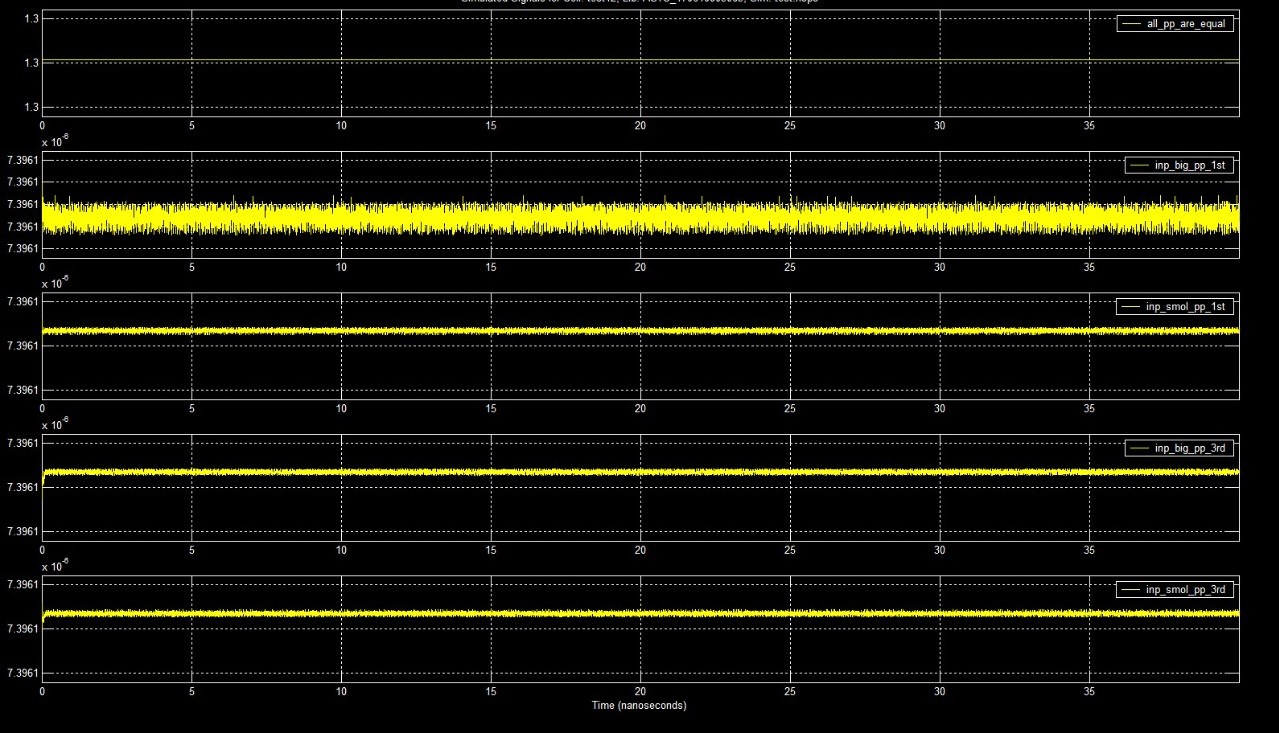


Figure: Comparator Output.

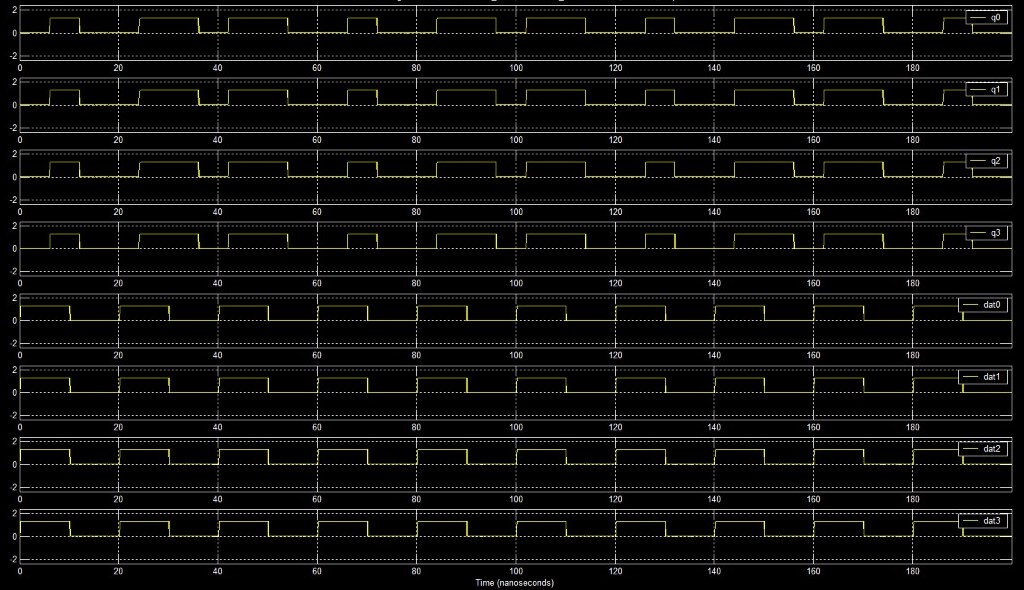


Figure: Speed Output.

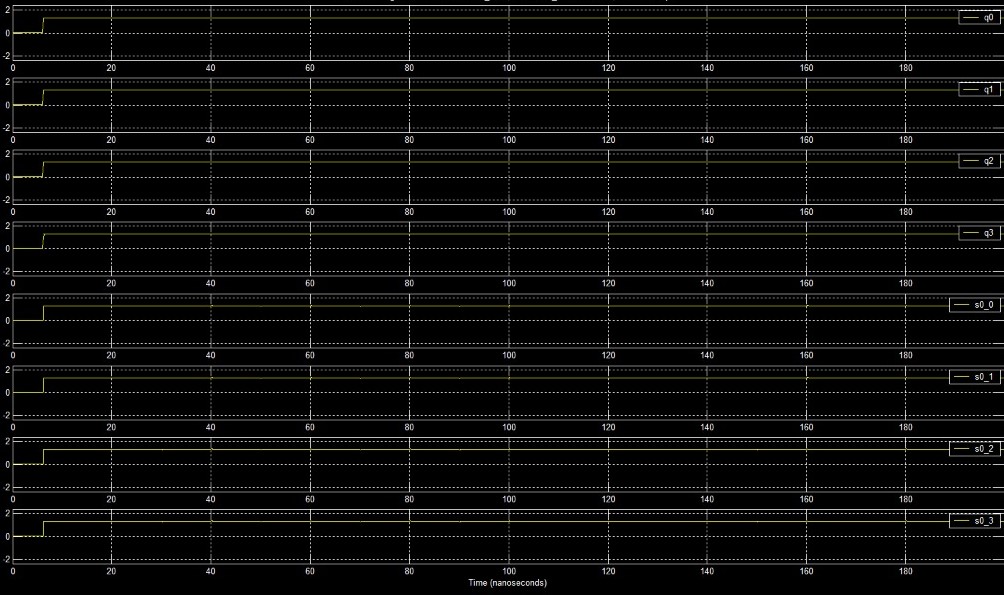


Figure: Brakes Output.